**DAILY ASSESSMENT FORMAT**

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| **Course:** | **VLSIdesign** | **USN:** | **4al16ec074** |
| **Topic:** | **MOSFET - Enhancement Type MOSFET Explained(Construction, Working and Characteristics Explained)** | **Semester & Section:** | **8-B** |
| **Github Repository:** | **shreya-test** |  |  |

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| **Image of session** |
| **Report**  **4:1 mux using pass transistor logic**    **Advantages of using transmission gate logic**   * A CMOS transmission gate can be constructed by parallel combination of nMOS and pMOS transistors, with complementary gate signals. * The main advantage of CMOS transmission gate compared to nMOS transmission gate is to allow the input signal to be transmitted to the output without the threshold voltage attenuation. * It allows full rail transition i.e. ratioless logic * The equivalent resistance is relatively constant during transition. * Some gates are efficient implemented using transmission gate.  **MOS Field-Effect-Transistors**  |  |  | | --- | --- | | **The linear model** |  |  |  | | --- | | The linear model describes the behavior of a MOSFET biased with a small drain-to-source voltage. As the name suggests, the linear model, describes the MOSFET acting as a linear device. More specifically, it can be modeled as a linear resistor whose resistance is modulated by the gate-to-source voltage. In this regime, the MOSFET can be used as a switch for analog and digital signals or as an analog multiplier. |  |  | | --- | | The general expression for the drain current equals the total charge in the inversion layer divided by the time the carriers need to flow from the source to the drain: |  |  |  | | --- | --- | |  |  |  |  | | --- | | where *Q*inv is the inversion layer charge per unit area, *W* is the gate width, *L* is the gate length and *t*r is the transit time. If the velocity of the carriers is constant between source and drain, the transit time equals: |  |  |  | | --- | --- | |  |  |  |  | | --- | | where the velocity, *v*, equals the product of the mobility and the electric field: |  |  |  | | --- | --- | |  |  |  |  | | --- | | Now assume that the charge density in the inversion layer is constant between source and drain. We also assume that the basic assumption described in section applies, namely that the charge density in the inversion layer equals minus the product of the capacitance per unit area and the gate-to-source voltage minus the threshold voltage: |  |  |  | | --- | --- | |  |  |  |  | | --- | | The inversion layer charge is zero if the gate voltage is lower than the threshold voltage. Replacing  the inversion layer charge density in the expression for the drain current yields the linear model: |  |  |  | | --- | --- | |  | (7.3.6) |  |  | | --- | | Note that the capacitance in the above equations is the gate oxide capacitance per unit area. Also note that the drain current is zero if the gate-to-source voltage is less than the threshold voltage. The linear model is only valid if the drain-to-source voltage is much smaller than the gate-to-source voltage minus the threshold voltage. This insures that the velocity, the electric field and the inversion layer charge density is indeed constant between the source and the drain. |  |  |  | | --- | --- | |  | | | **The quadratic model** |  |  |  | | --- | | The quadratic model uses the same assumptions as the linear model. However, this model allows the inversion layer charge to vary between the source and the drain. |  |  | | --- | | The derivation is based on the fact that the current is continuous throughout the channel. The current is also related to the local channel voltage, >I>VC. |  |  | | --- | | We now consider a small section within the device with width dy>/I> and channel voltage VC + VS. The linear model as described by equation, still applies to such section, yielding: |  |  |  | | --- | --- | |  | ) |  |  | | --- | | The drain-source voltage is replaced by the channel voltage. Both sides of the equation can be integrated from the source to the drain, so that *y* varies from 0 to the gate length, *L*, and the channel voltage *VC* varies from 0 to the drain-source voltage, *V*DS. |  |  |  | | --- | --- | |  |  |  |  | | --- | | The drain current, *ID*, is constant so that integration results in: |  |  |  | | --- | --- | |  |  |  |  | | --- | | The drain current first increases linearly with the applied drain-to-source voltage, but then reaches a maximum value. According to the above equation the current would even decrease and eventually become negative. The charge density at the drain end of the channel is zero at that maximum and changes sign as the drain current decreases. As, the charge in the inversion layer does go to zero and reverses its sign as holes are accumulated at the interface. However, these holes cannot contribute to the drain current since the reversed-biased p-n diode between the drain and the substrate blocks any flow of holes into the drain. Instead the current reaches its maximum value and maintains that value for higher drain-to-source voltages. A depletion layer located at the drain end of the gate accommodates the additional drain-to-source voltage. This behavior is referred to as drain current saturation. |  |  | | --- | | Drain current saturation therefore occurs when the drain-to-source voltage equals the gate-to-source voltage minus the threshold voltage. The value of the saturated drain current, *ID,sat*. is then given by the following equation: |  |  |  | | --- | --- | |  | (7.3.10) |  |  | | --- | | The quadratic model explains the typical current-voltage characteristics of a MOSFET, which are normally plotted for different gate-to-source voltages. An example is shown in Figure. The saturation occurs to the right of the dotted line which is given by *I*D = m *C*ox *W*/*L* *V*DS2. |      |  | | --- | |  | |